Miniaturization of high voltage MLCC for space applications

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INTRODUCTION

Miniaturization of equipment is a permanent challenge in the space field, for space and weight reduction. The challenge with high voltage components used in space application is a breakdown (surface arcing) that can appear at voltage below 350 V. To allow parts size reduction while maintaining optimal reliability and avoid surface arcing, varnishing or molding solutions exist for single leaded chips. For stacked MLCC however, the arcing risk remains in the areas between the chips elements, because of presence of gas.

Fig.1: Single chip leaded part

Fig. 2: Stack leaded part
(high cap for this example)

BREAKDOWN VOLTAGE IN LOW-PRESSURE GASEOUS ENVIRONMENT

According to the High voltage engineering and design handbook, the basic breakdown mechanism is caused by collision of charge carriers in the gas volume and interactions with the electrode surfaces (Townsend mechanism). In principle, the electrical field accelerates free electrons inside gas-filled gap. These accelerated electrons are colliding with gas atoms. If the kinetic energy of the electrons is high enough, they ionize gas atoms, releasing further electrons. An avalanche of electrons can grow towards the anode, while the ions moving in opposite direction collide with the cathode releasing new electrons. A well ionized, high conductive breakdown channel can develop in a time frame of a few microseconds. As a consequence of the avalanche breakdown, there is always an optimum, where molecule distance (given by gas pressure) and electrical field strength (given by total gap distance) are providing optimum conditions for ionisation. For these "optimum" conditions, the result is a very low breakdown voltage. This physical relation is expressed by the "Paschen Law" and the corresponding "Paschen Curve", which gives a breakdown voltage of 330 V. To mitigate this issue, an insulating material is applied on the surface of high voltage components.

To miniaturize a footprint, several capacitor chips can be stacked. In this case, you must be able to insure that there is no risk of arcing between the opposite poles, in the zones that cannot be protected by external potting.

EXXELIA SOLUTION TO PROPOSE SMALLER PARTS

The Exxelia's solution is the second one, stacking parts to reach in a smaller case the same capacitance as the one available in single chip bigger parts.
Exxelia manage for a long time parts stacking for space application (cf to CNC5x and CNC3x high capacitance QPL series), but on low voltage parts (high capacitance series have a maximum rated voltage of 500V) or on standard parts where insulation is not mandatory required everywhere around the parts.

Fig. 4: High capacitance QPL CNC5X series

For space application, the main point is to find a way to ensure this insulation everywhere in the stack, in particular between the chips.
Exxelia's solution needs an ''interchip'' filling material, which must be isolating, thermo-mechanically compatible with following steps of component finishing, for example lead frames soldering. It must also be compatible with customer's use of the component.

Lead frames soldering for space applications uses High Melting Point leaded alloy, with copper silvered DIL shaped lead frames ; the reflow temperature of this alloy is 310°C, and must be processed at 400°C for hand iron soldering, with preheating of the chips to prevent thermomechanical cracks. The filling material must be applied on the chips before stacking them, to be sure to insulate their surface. It means that the chosen material must be able to support the lead frames soldering process, preheating as well as solder reflow.

We choose a glass material to do this filling role. This glass is supplied as a paste, in jars that will be transfered in a syringe to be deposed by dispensing, and we choose to use the automatic dispensing via a 4 axis dispensing robot.

GLASS DEPOSITION - EXPERIMENTAL TRIALS

First task of this project was to find the adequate way of processing the glass paste, to create an efficient inter-chip insulating barrier. It includes:

- chips preparation : only one of the two chips to link ''glassed'', both surfaces to link to ''glass''
- glassing firing cycle definition : pre-firing on single chips needed (spread glass reflow cycle) or not, firing cycle definition (stacking=linking glass reflow cycle)
- tooling definition for the reflow = stacking cycle
- effect of glass filling (presence and quantity) on soldering step (stacking) and on thermomechanical behaviour of the stacks
- deposition parameters vs ink viscosity : robot cycle parameters, i.e. movements management, pressure management, syringe spindle,

1 – Deposition definition:

On one side, filling material is mandatory to increase electrical breakdown strength between opposite poles of the parts, and on the other side, if there is some leakage of filling material on ends terminations, it could affect lead frames soldering and/or contact efficiency (ESR…).

An automatic deposition way (Janome JR3000 deposition robot) has been chosen to ensure the reproducibility:

Fig. 5: 4 axis deposition robot

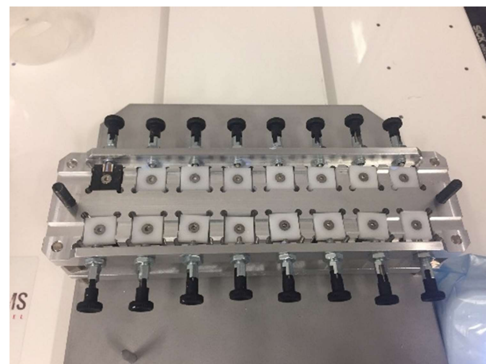

Fig. 6: Deposition maintaining tool

Glass material is a product previously used by Exxelia for a similar insulation application..

First trials aimed to fill totally the space between parts, with different deposition cycles (back and forth scanning movement, zig-zag movement, rectangular spiral movement…); the glass layer covers all the ceramic surface but flows on the edges of the parts.

One important point is too avoid glass to go on the end terminations, because it will affect the solderability and consequently the ''stackability'' of the parts. Previous internal studies have shown that every component of the stack (ceramic-end termination-solder-lead frames and also here filling material) has an impact on the thermomechanical behaviour of the stack. Most of the thermomechanical stresses occur on the end terminations; so glass presence in this area may change already known behaviour.

Exxelia previous stacking trials showed that it is very difficult to manage the glass paste deposit to optimise the glass layout and quantity after sintering.

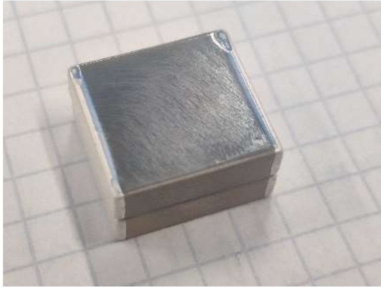

Fig. 7: Glass full-filled preliminary tests after sintering

One can see on pictures fig.7 that glass flows everywhere between the chips, particularly on the end terminations.

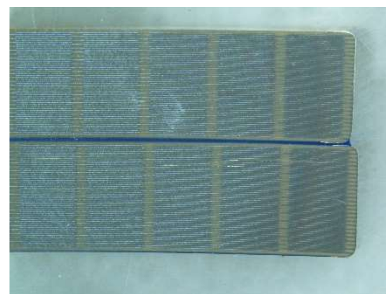

Fig. 8: Preliminary glass full-filling trials

These trials also showed that bending of the chips can affect glass filling repartition during sintering reflow (Fig. 8).

Because this insulation solution will be applied to multiple series (different sizes, thicknesses of capacitors,) the full-filled solution seems to be difficult to control.
That's why we decided to prevent the leakage by adding only a glass line, parallel to the end terminations, in the middle of the length of the parts (Fig.9).

Experimental tests will show if this single glass line is sufficient to prevent any arcing between opposite poles of the capacitors stack.

2 – Glass thermal treatment definition : parameters and tooling

Glass filling process is not only deposition but also thermal treatment of the material. Glass paste supplier technical data sheet advises to pre-sinter the glass layer on the first chip (burn out step), and to reflow a second time after stacking the chips together (adhesion step). This protocol has been followed for the preliminary full-filled tests (Fig.7 and 8).

For single line barrier tests, no pre-sintering step performed, we proceeded as follow:

- Deposition of the glass paste on one chip and stand by for 5 min (levelling step),
- Stacking of the second chip,
- Drying at 125 °C for 15 min,
- Burning-out and sintering of the glass, in a box oven, under air: 530 °C for 30 min,
- Free cooling.

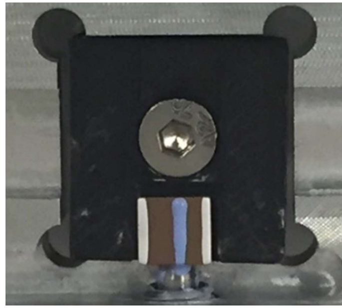

Fig. 9: 2220 size part after glass deposition

Fig. 10: 2 chips 2220 size stacked with line barrier

Electrical results detailed in the following section have been generated on parts similar to Fig. 10.

ELECTRICAL BEHAVIOUR SIMULATION

The aim of the study is to show pressure effect on withstanding voltage values, to validate/invalidate the Exxelia HV stacks useability for aeronautics and/or space applications. On a quite small part,2220 size, without any internal electrode (the aim here is to check external withstanding of the stacks and not internal withstanding of the dielectric), we tested withstanding voltage change between atmospheric pressure and a pressure of 200-250 mbar, which corresponds to an altitude between 10000 and 11500 meters (long flights cruise altitude). A low pressure measurement equipment has been developed in-house to generate the data.

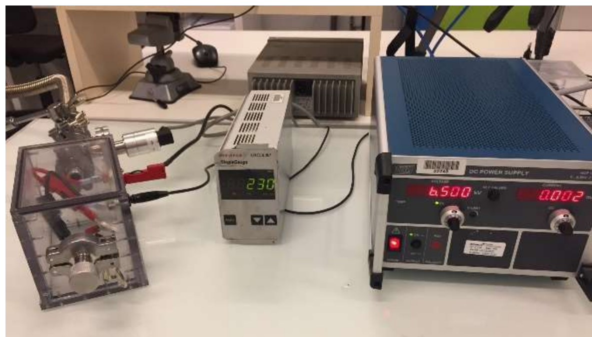

Fig. 11: Low pressure box measurement equipment

NB: Withstanding voltage meaning in the following tables is the minimum measured voltage at which there is no surface arcing => withstanding = still OK.

1 – Withstanding voltage reference (under atmospheric and low pressure) :

To fix reference values, we did the withstanding voltage measurement on 2220 single bare parts (without any barrier), under atmospheric pressure and under low pressure (220-240 mbar) range:

Table 1: 2220 bare single chip withstanding voltage values

Sample	Pressure value (mbar)	Withstanding voltage (V_{DC})	Pressure value (mbar)	Withstanding voltage (V_{DC})
1-1	atmospheric	> 6500	240	3300
1-2	atmospheric	> 6500	240	3100
1-3	atmospheric	> 6500	240	3400
1-4	atmospheric	> 6500	230	2500
1-5	atmospheric	> 6500	220	2200

The difference of withstanding voltage is significant: from 6500 V_{DC} at atmospheric pressure to 2200 V_{DC} at lower pressure.

2 – Influence of glass barrier presence on withstanding values :

On the same parts as paragraph 1, some stacks of two chips have been manufactured, with glass line barrier (parts 2-1 to 2-5) vs no barrier stacks (parts 2-6 to 2-10), and all externally covered with a silicone varnish (aerosol deposition) to simulate customer potting (external leakage prevention). Only low pressure measurements have been performed.

Table 2: Withstanding voltage on 2220 varnished stacks with vs without glass barrier

Sample	With glass barrier / No barrier	Pressure value (mbar)	Withstanding voltage (V_{DC})
2-1	With glass barrier	250	> 6500
2-2	With glass barrier	260	5000
2-3	With glass barrier	210	5500
2-4	With glass barrier	230	4000
2-5	With glass barrier	230	4000
2-6	No barrier	240	2500
2-7	No barrier	220	4000
2-8	No barrier	240	2800
2-9	No barrier	230	3500
2-10	No barrier	230	3500

Withstanding voltage values are globally higher on stacks with glass barrier than without.

Another run of trials has been performed on similar 2 chips stacks, with glass barrier or not, with no varnish, to try to localize the leakage when occurring, with insulation of the end terminations:

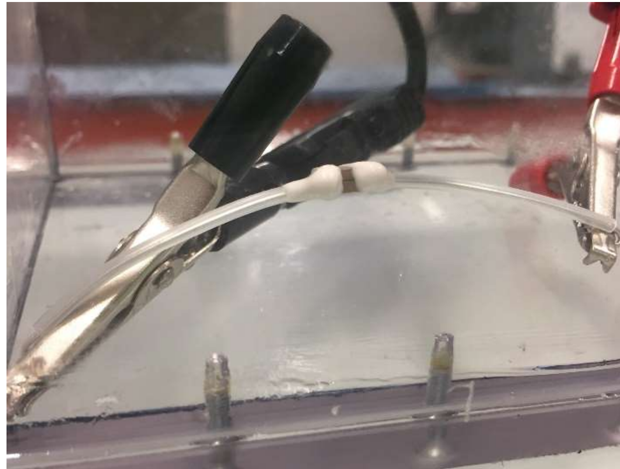

Fig. 12: Low pressure measurement on 2 chips stack

Table 3: Withstanding voltage on 2220 unvarnished stacks, end terminations covered, with vs without glass barrier

Sample	With glass barrier / No barrier	Pressure value (mbar)	Withstanding voltage (V_{DC})	Comments
3 -1	With glass barrier	210	4000	Glass surface arcing*
3 - 2	With glass barrier	200	> 6500	NA
3 - 3	With glass barrier	210 21	> 6500 2000	NA Arcing between measurement clamp
3 - 4	With glass barrier	200	4500	Glass surface arcing*
3 - 5	With glass barrier	220	2500	Glass surface arcing*
3 - 6	With glass barrier	220	> 6500	NA
3 - 7	With glass barrier	210	> 6500	NA
3 - 8	With glass barrier	220	4500	Glass surface arcing*
3 - 9	With glass barrier	220	> 6500	NA
3 - 10	With glass barrier	200	3500	Glass surface arcing*
3 - 11	No barrier	210	5000	Arcing between chips
3 - 12	No barrier	210	3000	
3 - 13	No barrier	220	3000	
3 - 14	No barrier	210	3000	
3 - 15	No barrier	210	2500	
3 - 16	No barrier	190	3000	
3 - 17	No barrier	240	3500	
3 - 18	No barrier	240	4000	
3 - 19	No barrier	230	5000	
3 - 20	No barrier	240	4000	
3 - 21	No barrier	220	3000	

* the arcing on the surface of the glass occurs on the side of the stacks: the electrical arc goes around the glass barrier.

It is clear with this measurement configuration that glass barrier is efficient. The low pressure withstanding values of stacks with the glass barrier (parts 3-1 to 3-10, table 3) are similar to the reference ones at atmospheric pressure (parts 1-1 to 1-5, atmospheric values, table 1): no breakdown till maximum voltage delivered by test equipment (6500 V_{DC}). On some parts, a leakage occurred at the surface of the glass (unvarnished surfaces on the sides of the stacks), which wouldn't occur with an external potting.
Very low pressure measurement performed on part 3-3 (21mbar) also shows that it's efficient for space conditions environment: the arcing occurred between the clamps and not on the parts.

It means that the glass line deposed between the opposite poles acts as planned as a protective barrier, which improves breakdown voltage of the stack under low pressure.

CONCLUSION

Exxelia's solution to manufacture reliable HV stacks useable in aeronautics and space conditions seems to work regarding presented results. It is a promising technology to decrease capacitor footprints in space applications.

Exxelia is performing additional studies (including CSAM observations) to confirm this technology on various configurations (ceramics, sizes and thicknesses of the chips) and, also, on functional HV parts (with electrodes) before qualification and release to customers.